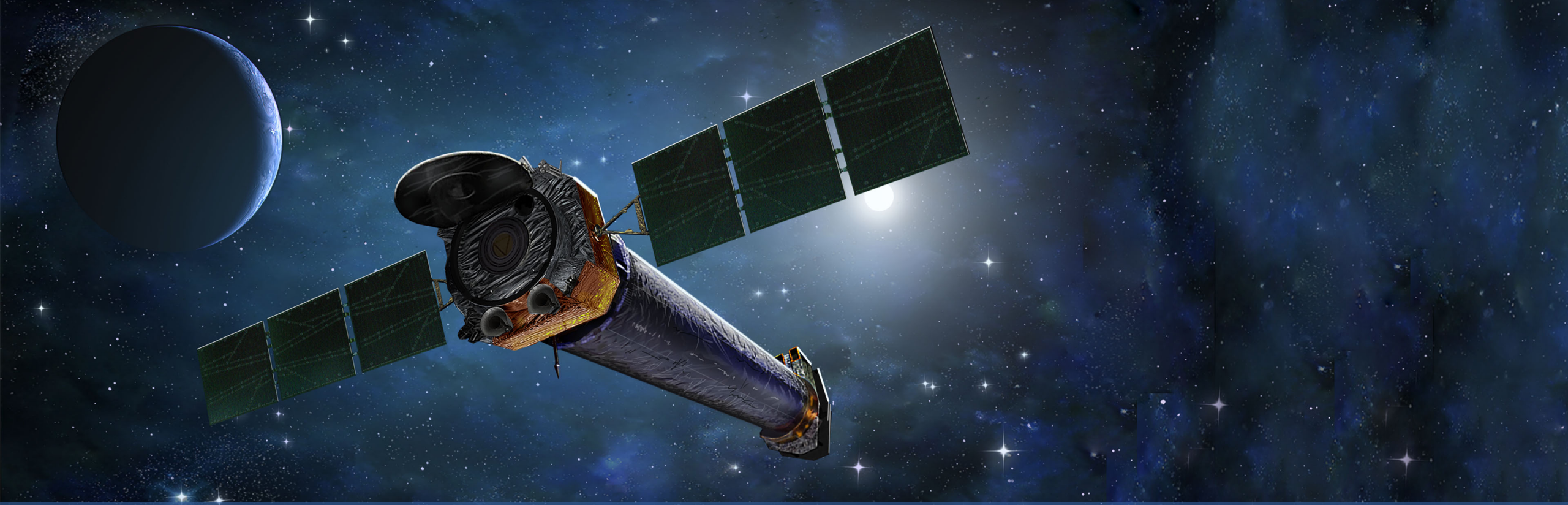


2022 HRC Anomaly Status – CUC Briefing

Dan Patnaude

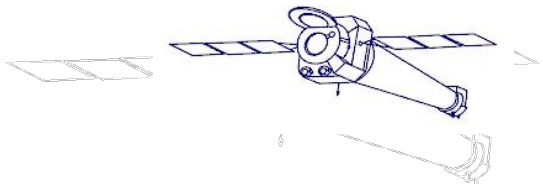
11/28/2022

Context – Current Status of the HRC

- The HRC is currently powered by the +5V LVPS on the side-A electronics. The ±15V LVPS and anticoincidence shields remain powered off unless the HRC detectors are actively taking science data

HRC Checkout Observations

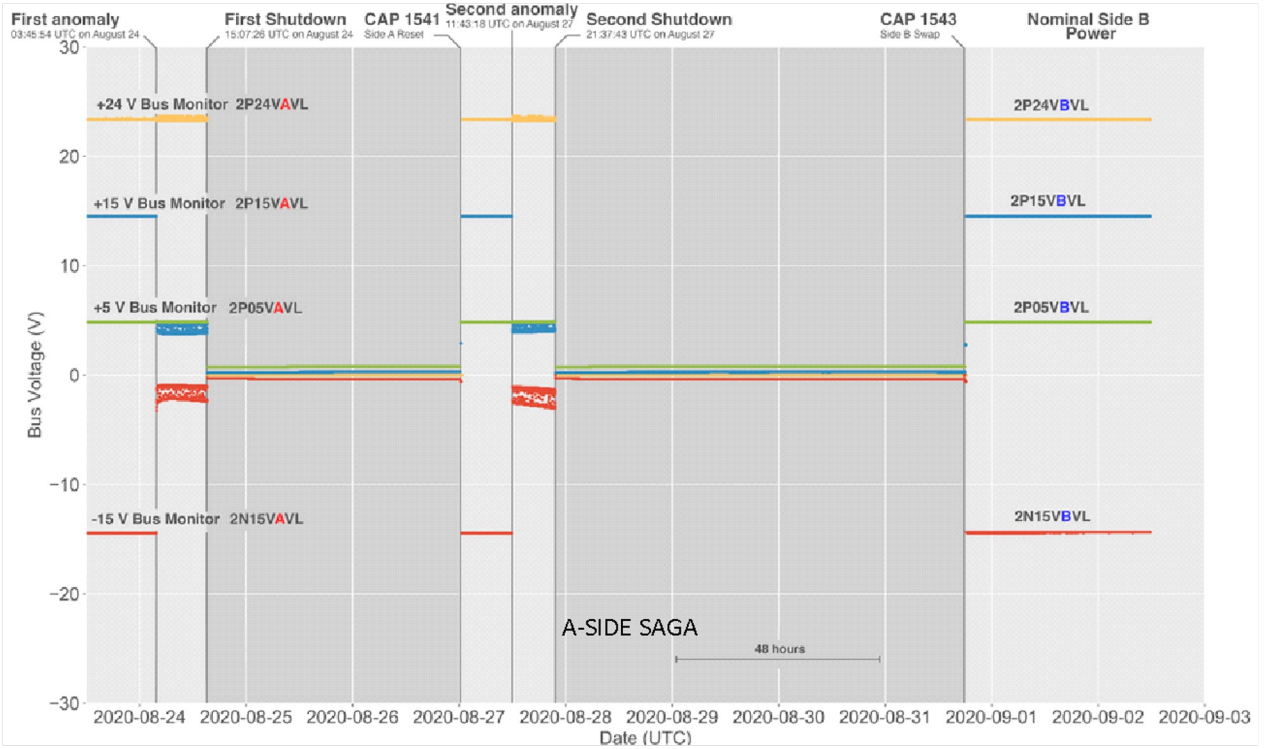
- Four HRC observations were conducted between June and September
  - Two HRC-I and two HRC-S of increasing duration at different satellite attitudes
  - An operational limit of 10C on MSID 2CEAHVPT was imposed for all observations
    - The thermistor associated with MSID 2CEAHVPT is located close to the LVPS board in the HRC CEA. It provides a suitable proxy for the LVPS board temperature (2LVPLATM) which is otherwise only available while the ±15V LVPS is powered on and functioning nominally – a plot which shows that 2CEAHVPT tracks 2LVPLATM is included in the supplemental material
    - All observations approached 10C, but none crossed this threshold
  - The last observation was for 15ks – moving forward, upcoming HRC activities will have a maximum duration of 15ks
    - As confidence is gained in the thermal model used for planning purposes, this duration restriction may be relaxed
- Science and engineering data were deemed to be nominal both in real time and as part of post-processing analysis
  - Secondary science corruption was observed in all four observations but does not impact the quality of the primary science data
    - Secondary science corruption has been present in side-A HRC observations since early in the mission – procedures are in place to account for it and to instruct observers on how to correct for it
  - Results from first two checkout observations are shown in supplemental material – second two checkout activities included GO observations and the data are proprietary – data appeared nominal



HRC Anomalies – Summary

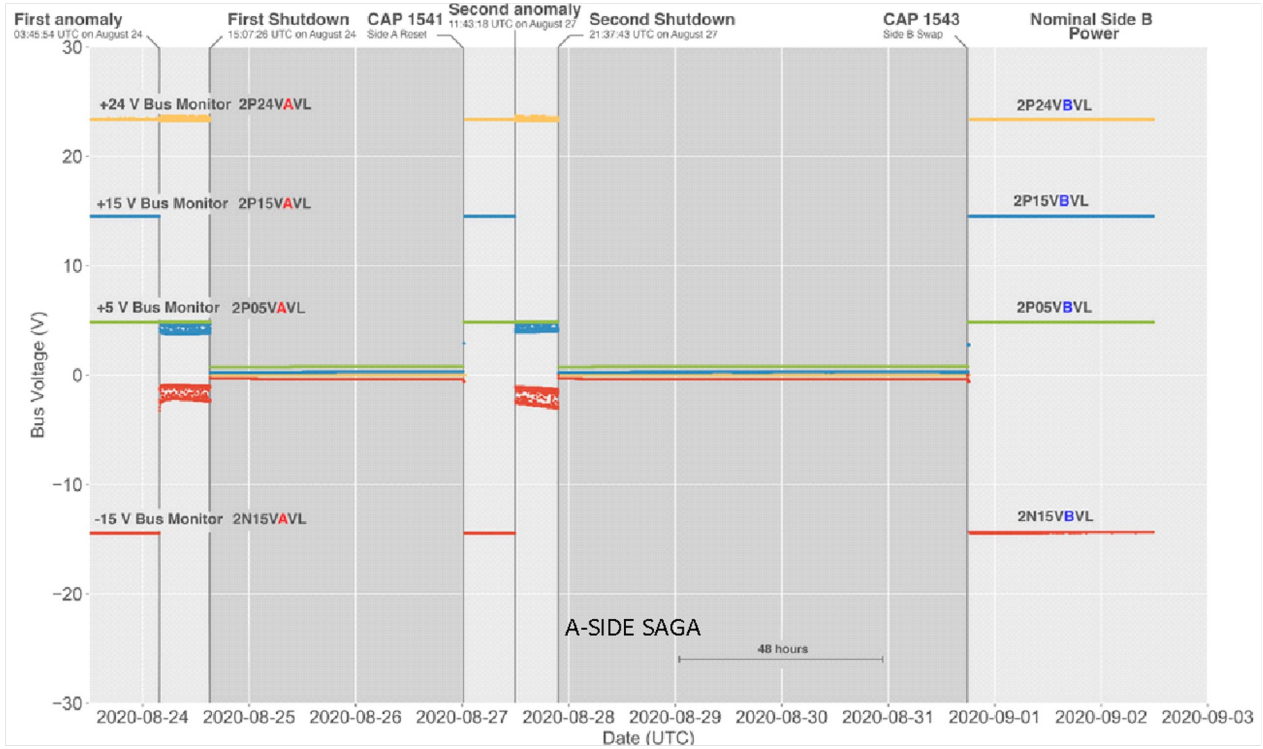
HRC Anomalies – Electrical and Thermal Summary

- Side-A Anomaly – A1 (August 25, 2020):
  - Anomaly state A1:
    1. ±15V voltage magnitudes out of spec with LOW values
    2. ±15V buses exhibited high noise levels
    3. -15V level appeared to slowly trend back towards a higher value
    4. All SSD telemetry went out of spec due to a loss of analog power to secondary science data processors
    5. CEA was at normal operating temperatures (~ 25C) prior to entering the anomalous condition
    6. FEA temperatures dropped, while CEA temperatures rose
  - Assumed a single event latchup and performed a restart
    - System operated for several hours before re-faulting with nearly identical symptoms



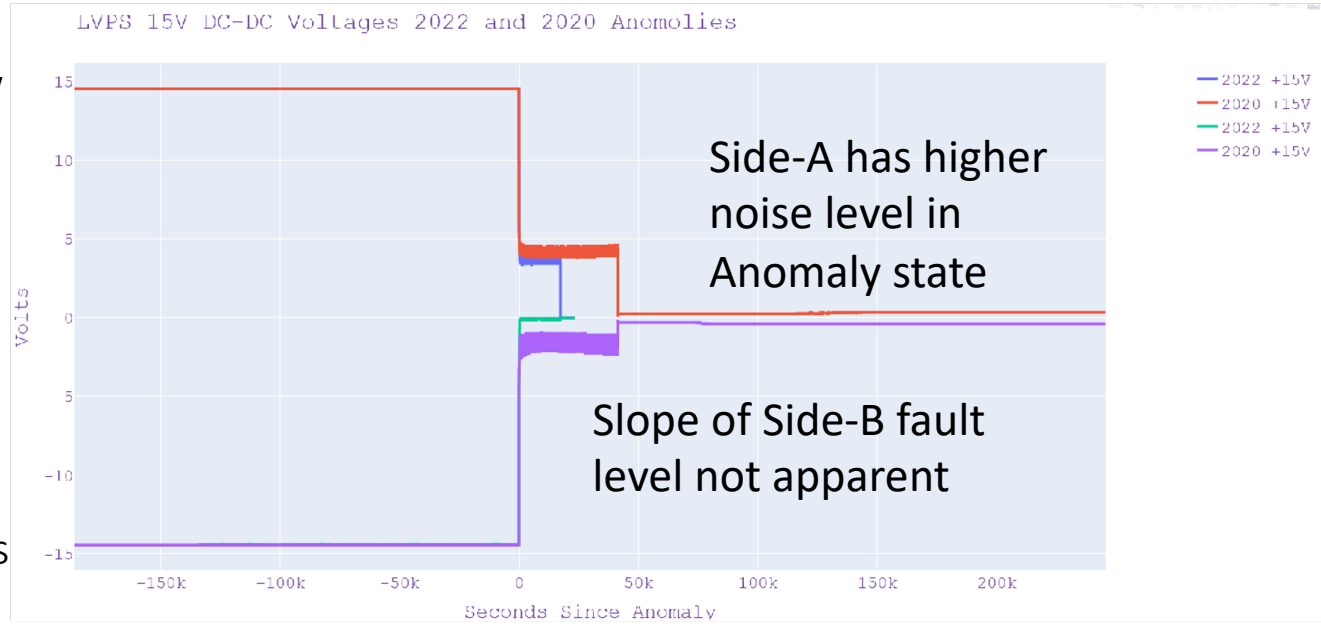
HRC Anomalies – Electrical and Thermal Summary

- Side-A Anomaly – A2 (August 27, 2020):
  - Anomaly state A2:
    1. ±15V voltage magnitudes out of spec with LOW values
    2. ±15V buses exhibited high noise levels
    3. -15V level appeared to slowly trend back towards a higher value
    4. All SSD telemetry went out of spec due to a loss of analog power to secondary science data processors
    5. CEA started cold and rose to a temperature of 12C before returning to the anomalous state
       - Remained in the anomalous state for approximately 11 hours
    6. FEA temperatures dropped, while CEA temperatures rose
  - Return to the faulted state on Side-A led the team to power down and perform a swap to Side-B



HRC Anomalies – Electrical and Thermal Summary

- Side-B Anomaly – B1 (February 9, 2022):
  - Anomaly state B1:
    1. ±15V voltage magnitudes out of spec with LOW values
    2. +15V bus exhibited a “two-step” behavior – rapid drop to ~ 4.5V followed by a decrease to 3.5V
    3. -15V level also exhibited a “two-step” drop
       - The two-step drop is interpreted as the inverting op-amplifier stage shutting down due to low +V
    4. All SSD telemetry went out of spec due to a loss of analog power to secondary science data processors
    5. CEA was at normal operational temperatures prior to entering the anomalous state
    6. FEA temperatures dropped, while CEA temperatures rose
  - Attempted a restart of the Side-B, which was unsuccessful (March 11, 2022)



HRC Anomalies – A/B Comparison

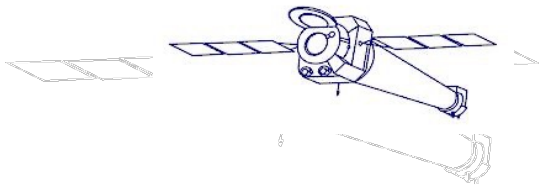
Parameter	SIDE-A	SIDE-B	COMMENT
+15V TM	LOW (~4V)	LOWER (~4.5V → 3.4V , 2-step)	Possible secondary failure on side-B
-15V TM	LOW (~-2.3V)	LOW (~-2.3V, drop to 0V)	Op amp shutdown on side-B shows 0V for –V EED TM
NOISE	YES	YES	Likely due to converter switching noise, trying to close loop
Slope on Faulted Levels	Yes, picks up same point on re-fault	Not obvious due to shorter time in anomalous state	This has not been fully investigated
RESTART	YES, Repeatedly	NO (ENABLES in FAULT)	
FEA TEMP	COLD	COLD	±15V provides 90% of the power to FEA DC-DC converter load fault power diss. Is 10W typ. Per Data sheet
CEA TEMP	HOT	HOT	

Sec +5V Bus A (V)	4.88
Sec +15V Bus A (V)	4.14
Sec -15V Bus A (V)	-2.34
Sec +24V Bus A (V)	23.51

A-Side Anomaly

+5V LVPS B (V)	On
Sec +5V Bus B (V)	4.88
Sec +15V Bus B (V)	3.36
Sec -15V Bus B (V)	-0.16
Sec +24V Bus B (V)	23.51

B-SIDE Anomaly (RTCADS)



HRC AWG – Root Fault Analysis and Recommendation

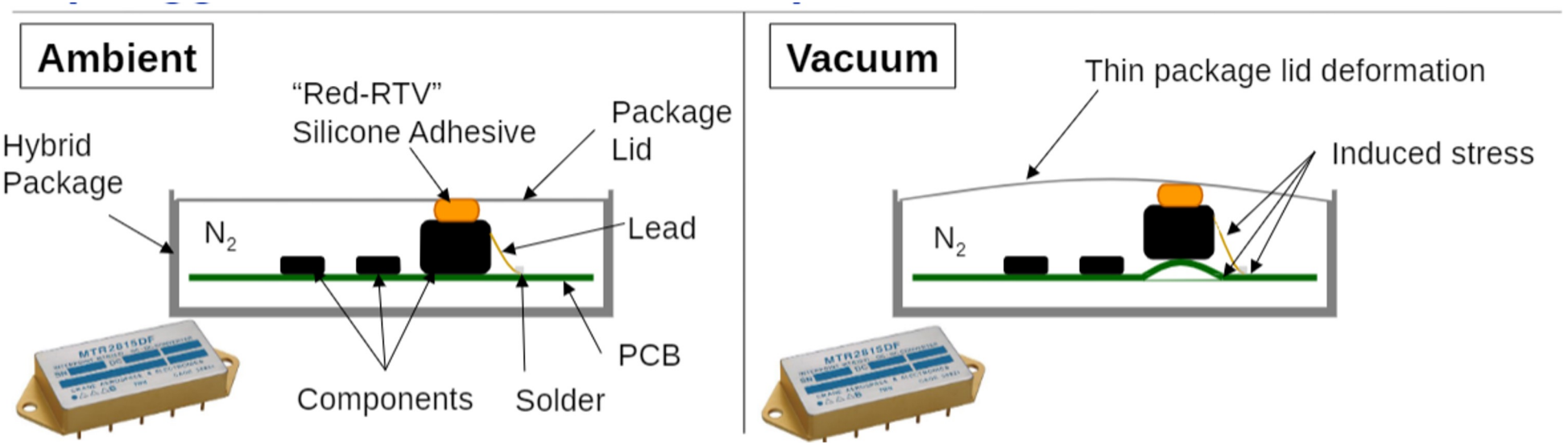
HRC AWG – Root Fault Analysis – Summary

- Root fault analysis indicates two possibilities
  - MTR2815F DC—DC converter
    - Previous failures identified (GSFC Report No. FA99695)
    - Root cause believed to be solder joint failure due to bulging of package lids under vacuum conditions with additional strain due to internal component heating. Some internal solder joints from magnetics to internal board are not sufficiently strain-relieved
  - Multi-Layer Ceramic Capacitor (MLCC) 50V, 1µF (M39014/02-1419)
    - There is one of these from each MTR2815D converter output in the CEA to filter out switching noise. There is no current limiting resistor in place
    - Suspected shorting between plate layers due to “whisker” growth
    - Flagged by NASA and limited approval to 0.47µF value parts

- A complete report on HRC AWG activities and current findings will be presented at a separate briefing to be scheduled at a future date

HRC AWG – Component Root Fault Analysis

- MTR2815DF DC—DC converter
  - Entered NDA with CraneAE for disclosure of MTR28D design details
  - CraneAE provided:
    - Engineering support via phone/web
    - Bench testing of de-lidded contemporaneous converter
    - Testing included opening specific connections corresponding to suspect joints, while unit under load
    - A complete SPICE model was created – simulations were performed for each suspected failure mode



J.M.

— note: material presented on this page is not subject to NDA

HRC AWG – Component Root Fault Analysis

- MTR2815DF DC—DC converter

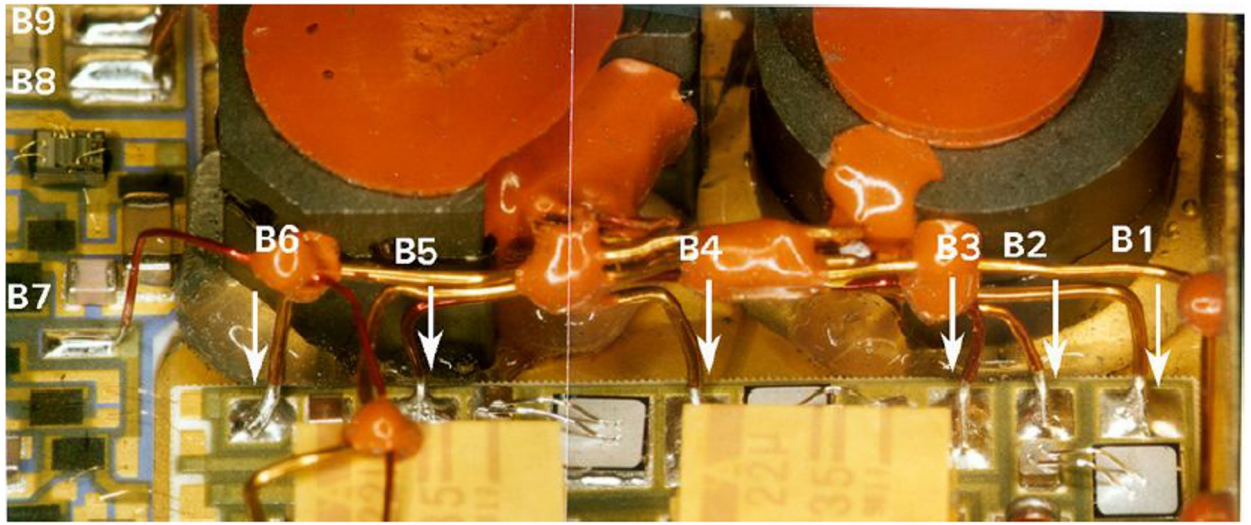


Figure 15. Overall internal view showing different solder joints. Note a lack of stress relief at bonds B3 and B6.

De-lidded MTR part showing internal magnetic components wired to carrier board - some with poor strain relief.

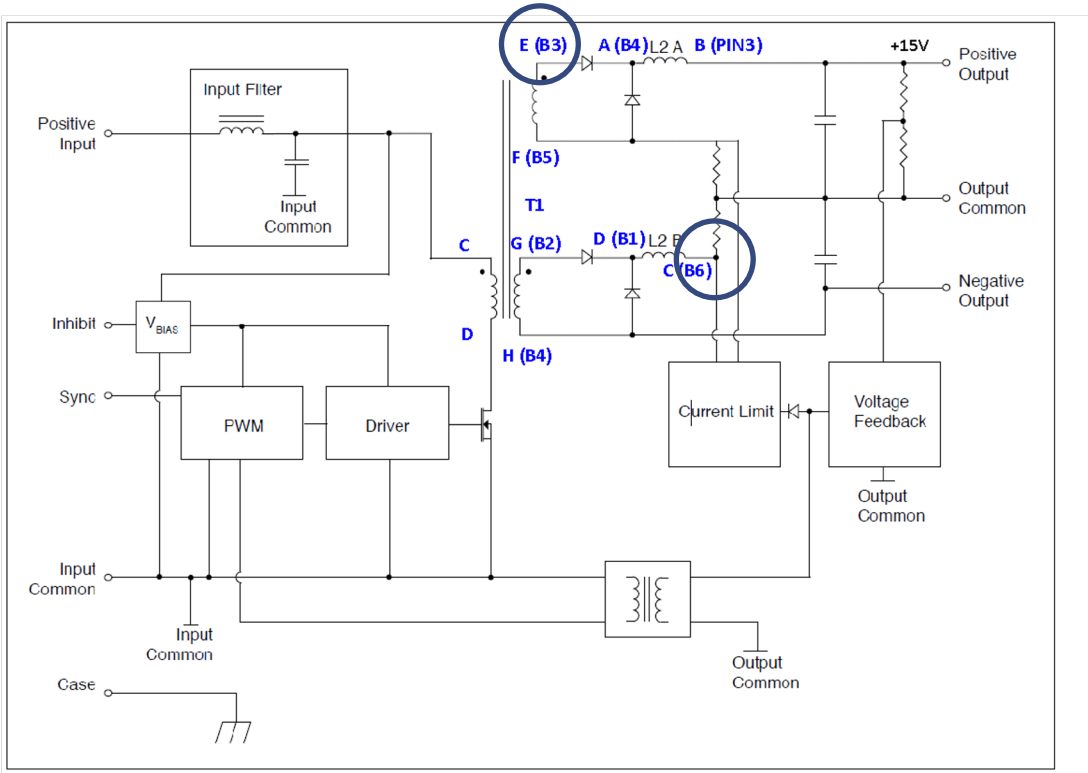


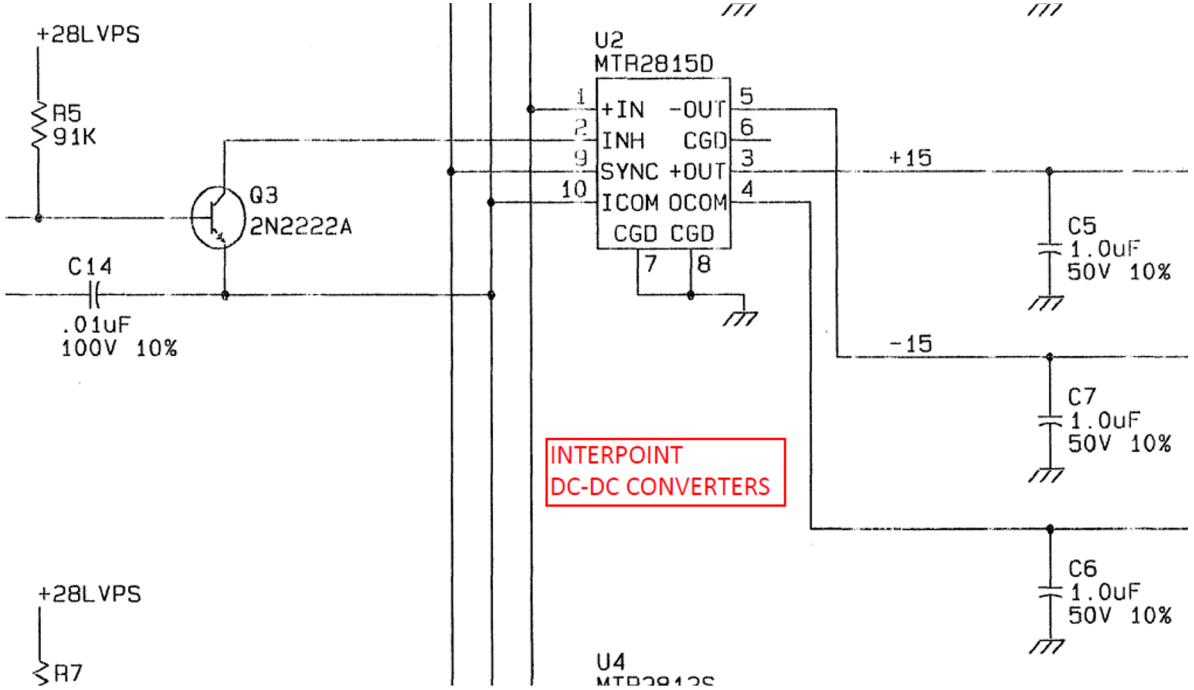
FIGURE 2: MTR DUAL /883 BLOCK DIAGRAM

Crane-Interpoint MTR Dual DC-DC converter Block Diagram w/references to device solder joint locations in previous figure. From: MTR (40 Series Datasheet) – Solder joints B3 and B6 circled

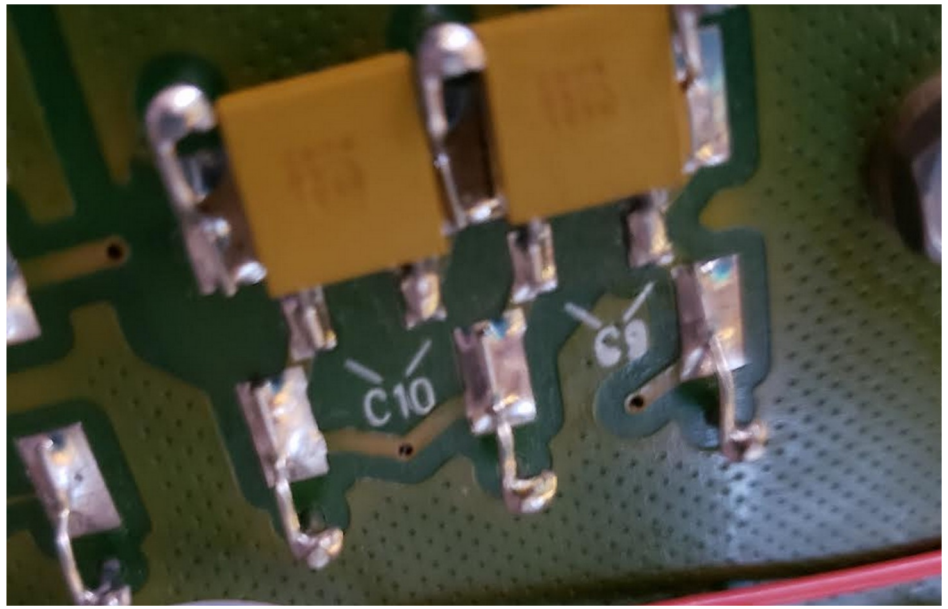
— note: material presented on this page is not subject to NDA

HRC AWG – Component Root Fault Analysis

- Multi-Layer Ceramic Capacitor (MLCC) 50V, 1µF (M39014/02-1419)
  - There is one of these from each MTR2815D converter output in the CEA to filter out switching noise. There is no current limiting resistor in place



From: HRC-5299 LVPS



MLCC's on EM LVPS PWA

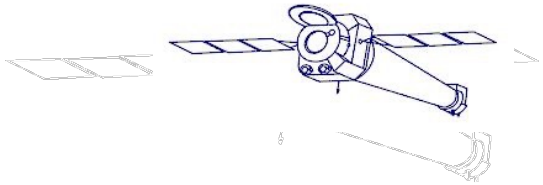
HRC AWG – Root Fault Analysis – Narrative Summary

- Root fault analysis included the following:
  - Identification of all components on the ±15V power buses
  - Systematic scoring of failure probability of each component on power buses based on the following criteria:
    1. Presence of current limiting resistors on associated power bus
       - Behavior of carbon CL resistors (in vac) under relevant high current conditions was tested
    2. Functionality of each component – based on telemetry – during period of Side-A restart
       - We did not operate the detector analog processing electronics (FEA preamplifiers) during this period
    3. Extensive thermal analysis and testing on EM using simulated power faults at locations within the CEA and FEA
    4. Study of prior failures of components within the system
  - Fault analysis score sheets are provided as supplemental material
- Current assessment:
  - No parametric shift in FEA components (as evidenced by side-A test observations) suggests root cause of anomaly is located in ±15V LVPS components
  - AWG electrical analysis shows with high confidence that the failure occurred in either the DC-DC converter or the MLCC
    - A preponderance of evidence indicated that the DC-DC converter is the more likely candidate
    - We have as of yet been unable to determine the specific failed sub-element with high confidence due to limitations in our available telemetry and testing, but have identified several candidate sub-elements.

HRC AWG – Recommendation for Return to Science

Based upon *current* findings, the HRC Anomaly Working Group recommends the following:

Given that the A-side anomaly re-occurred after the CEA heated to above 12C, the HRC should be operated with thermal constraints in place such that critical components do not heat above temperatures where a known failure has occurred. Additionally, minimum durations between HRC activities shall be set such that critical components can cool down. HRC cooling is currently not well characterized, suggesting a conservative lower limit on the cooling time



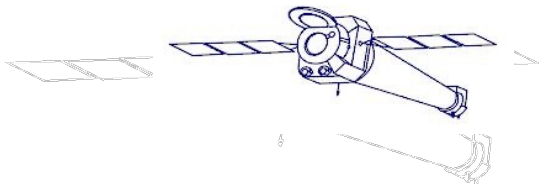
Changes to HRC Operations

HRC Operations – Planning Guidelines

- A new HRC operations paradigm has been developed based on experience with four HRC checkout observations
- New Mission Planning Guidelines (Priority definitions included in supplemental material):
  1. HRC CEA Thermal Planning Limit (Priority 1)
     - The predicted HRC CEA temperature (2CEAHVPT) as determined by FOT Matlab tools must not exceed +10 deg. C while the ±15V LVPS is powered on
  2. Maximum HRC On-time duration (Priority 1)
     - The duration from powering on the HRC ±15V to powering off the HRC ±15V must not exceed 15ks
  3. Minimum HRC Off-time duration (Priority 2)
     - The duration from powering off the HRC ±15V to powering on the HRC ±15V must not be less than 30ks

HRC Operations – Operational Changes

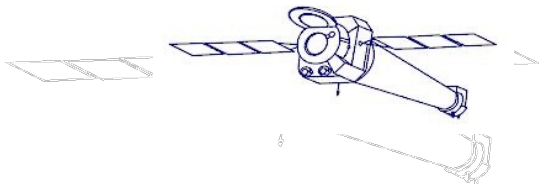
1. During ACIS cold ECS measurements, the HRC-S will be positioned at the focus position, but there will be no HRC-specific commanding. Accomplished via a SAR – to be converted to a planning guideline
2. No HRC stowed background data
3. No data from the HRC anticoincidence shield while the HRC is not operational
   - Note that ACIS will provide RADMON capabilities during HRC observations. RADMON triggers will be provided by the ACIS txings algorithm, which remains fully functional during Event Histogram runs (which is the typical configuration for ACIS while in format 1 when HRC is conducting science operations)
   - ACIS has built 2 CCD (one FI and one BI) Event Histogram SIMODES which can be selected by FOTMP in order to minimize the heat load on the HRC electronics during HRC operations
     - These new SIMODES have the value-added benefit of keeping ACIS electronics cooler during HRC observations



HRC Return to Science

HRC Return to Science

- Given the large number of SOT and FOT related products which need to be developed or updated, HRC return to science is targeted for mid-February, 2023
- An HRC Return to Science Working Group has been established to ensure all products are developed, tested, and approved in a timely manner

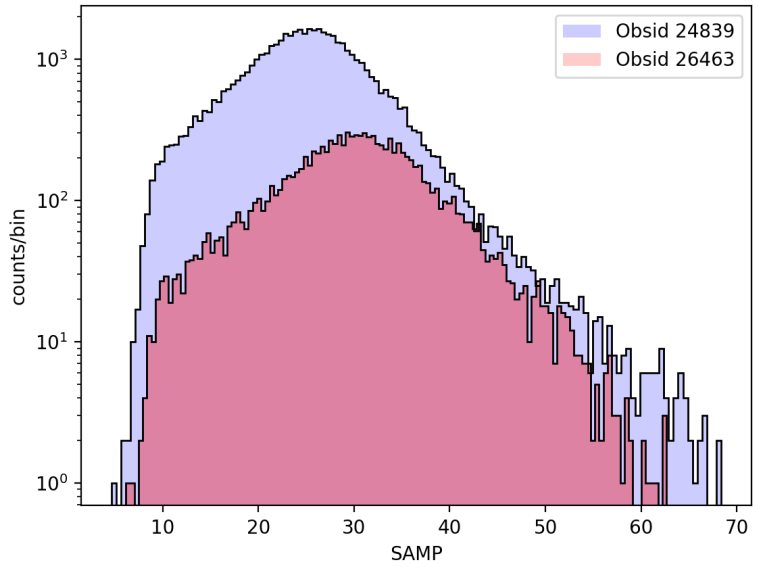


Supplemental Material

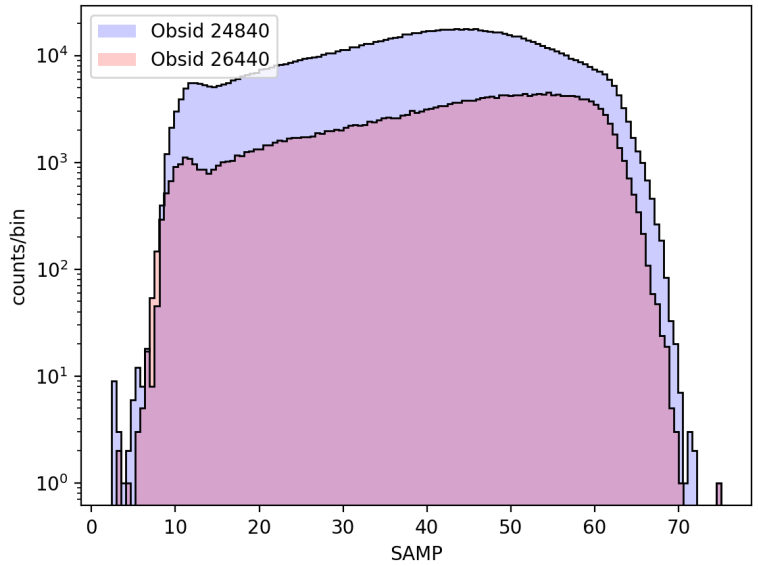
Supplemental Material

1. Comparative results from first two HRC checkout activities
2. AWG test results
3. Mission Planning Guideline Priority Definitions
4. HRC thermal model
5. List of SOT/FOT products requiring changes (and current status)

HRC Checkout Observations



- First checkout observation of Capella (HRC-S)
  - PHA and SAMP (a derivative of PHA and amplifier scaling factor) show that signal distributions are consistent with pre side-B anomaly
  - Shift to higher SAMP is a result of Spring 2021 HRC-S HVPS increase
  - SAMP distribution has not been normalized for difference in exposure times



- Second checkout observation of Capella (HRC-I)
  - PHA and SAMP (a derivative of PHA and amplifier scaling factor) show that signal distributions are consistent with pre side-B anomaly
  - Shift to higher SAMP is a result of Spring 2021 HRC-I HVPS increase
  - Cas A source spectrum is much harder than Capella – a qualitatively different shape is expected
  - SAMP distribution has not been normalized for difference in exposure times

HRC AWG – MTR Lab Tests and Simulations

FAILURE MODE	EXPECTED EFFECT	PREDICTED RELEVANT TM	COMMENT
1. MTR -V internal OPEN Solder Joint B6	+15V NOM, -15V OPEN Verified by test at CraneAE and SPICE at SAO	+15V EED NOM, -15V EED LOW	**+15V EED TM doesn't support this mode in either Side-A or Side B failures (A/B)**
2. MTR +V internal OPEN Solder Joint B4	+15V OPEN -15V max -26V Verified by test at CraneAE and SPICE at SAO	+15V EED LOW ~ +3.5V -15V EED LOW – due to op-amp shutdown Possibly, +5V leakage sufficient to allow bus V limited –V TM	+5V TM NOM, +5V leaks to +15V bus in FM / EM TM and in EM Lab tests indicate -15V current goes to +5V bus via ??? path
2A. MTR +V internal OPEN w/ subsequent ZD failure (SC) on -V to COM Solder Joint B4 & ZD SHORT	+15V OPEN -15V max V Verified by test at CraneAE and SPICE at SAO	+15V EED MED ~ +5V -15V EED LOW – due to op-amp shutdown Possibly, +5V leakage sufficient to allow bus V limited –V TM	**+15V EED TM doesn't support this mode in either Side-A or Side B failures (A/B)** Model suggests that –V current through dual inductor output filter couples energy to +V circuit to produce intermediate output voltage

HRC AWG – MTR Lab Tests and Simulations

FAILURE MODE	PREDICTED EFFECT	PREDICTED RELEVANT TM	COMMENT
3. MTR +V internal open at transformer sec + winding. ZD intact Solder Joint B3	+Vo at ~NOM value in SPICE sim (unexpected) -V and COM level shifted POS by several volts	Expected result - similar to 2A	+15V EED TM doesn't support this mode in either Side-A or Side B failures (A/B)
4. MTR -V internal open at transformer sec -V winding. ZD intact Solder Joint B2	+Vo at ~NOM value in SPICE sim (unexpected) -V and COM level shifted POS by several volts		

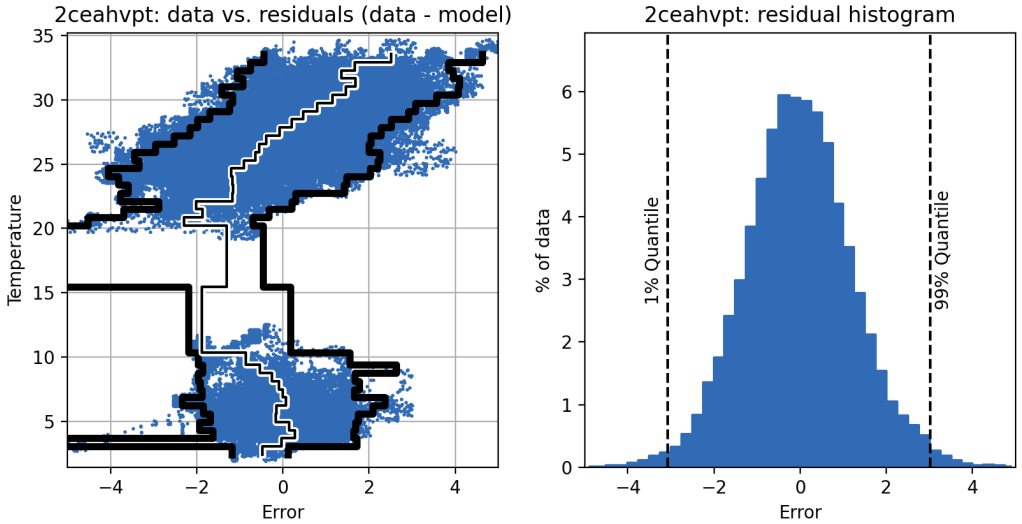
HRC AWG – MLCC Lab Tests and Simulations

FAILURE MODE	EXPECTED EFFECT	RELEVANT TM	COMMENT
1. +15V MLCC Low-R	+15V LOW -15V <NOM	+15V EED LOW, -15V EED LOW (A) +15V EED LOW, -15V EED LOW/0 (B)	A-side failure supports this since op-amp value for -15V should be lower then +V value -15V EED is suspect due to op-amp shut down due to low +V bus voltage
2. -15V MLCC Low-R	+15V LOW, -15V LOWER	+15V EED LOW, -15V EED LOW (A) +15V EED LOW, -15V EED LOW/0 (B)	A-side failure TM supports this with -15V op-amp marginally operating on low +V bus B-Side failure -15V EED TM suspect drop out This was our second leading theory

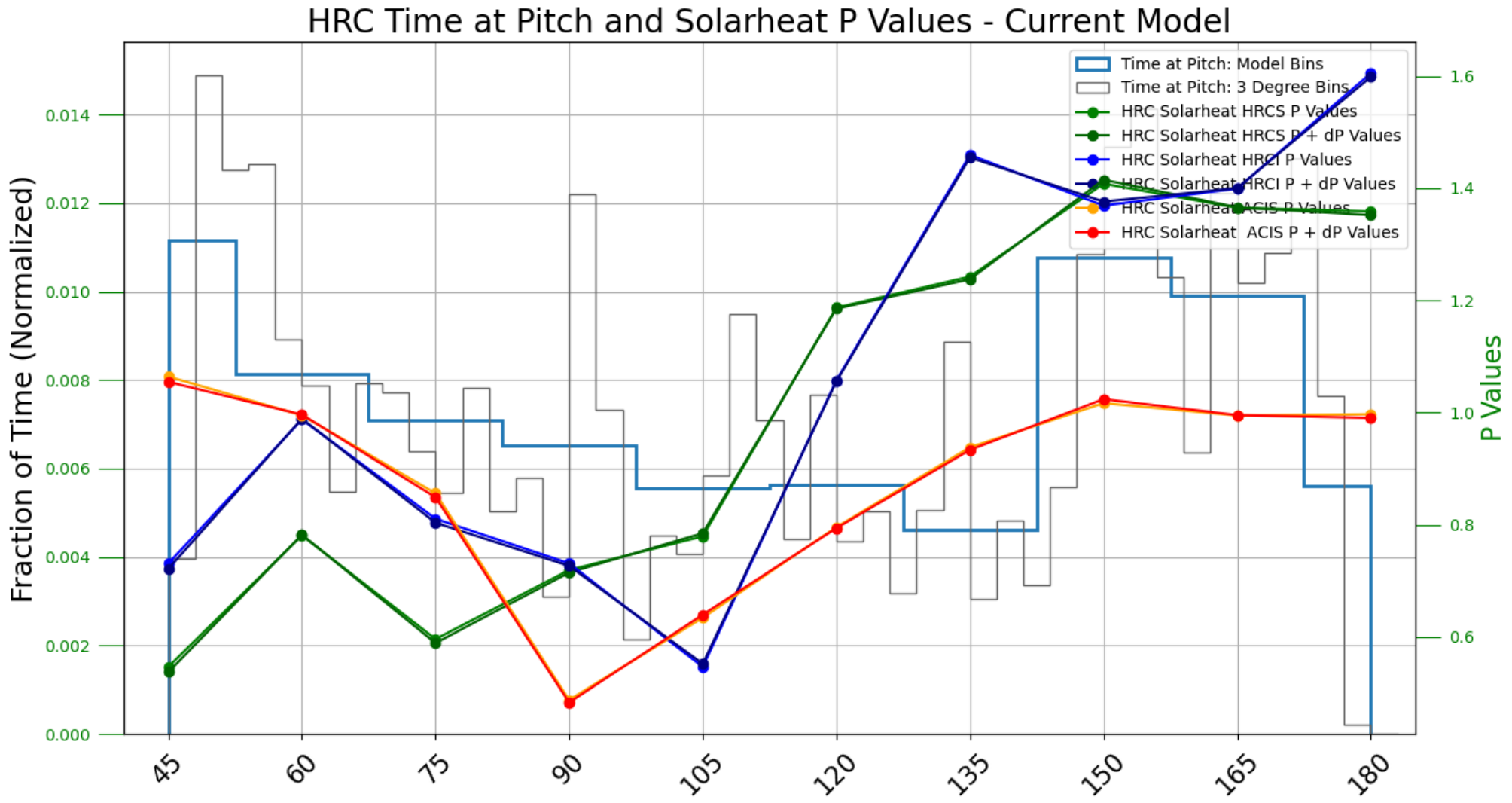
Mission Planning Guideline Priority Definitions

- **Priority 0:** Failure to meet guideline endangers immediate spacecraft health and safety or has high probability of causing Safe Mode. CARD constraints fall into this category
- **Priority 1:** Failure to meet guideline may cause Safe Mode or may cause acute degradation to a critical spacecraft component. CARD restrictions fall into this category
- **Priority 2:** Failure to meet guideline may cause safing action or cause long term degradation to a critical spacecraft component or system that could exceed operational life limits. CARD restrictions fall into this category.
- **Priority 3:** Failure to meet guideline jeopardizes the primary science objectives of an observation. CARD limitations fall into this category
- **Priority 4:** Failure to meet guideline may result in reduced efficiency, additional complexity of operations or data processing, contribute to long term degradation or increase the rate of use of life limited items.
- **Priority 5:** Meeting these guidelines provides additional benefit to the program or an observer above and beyond requirements

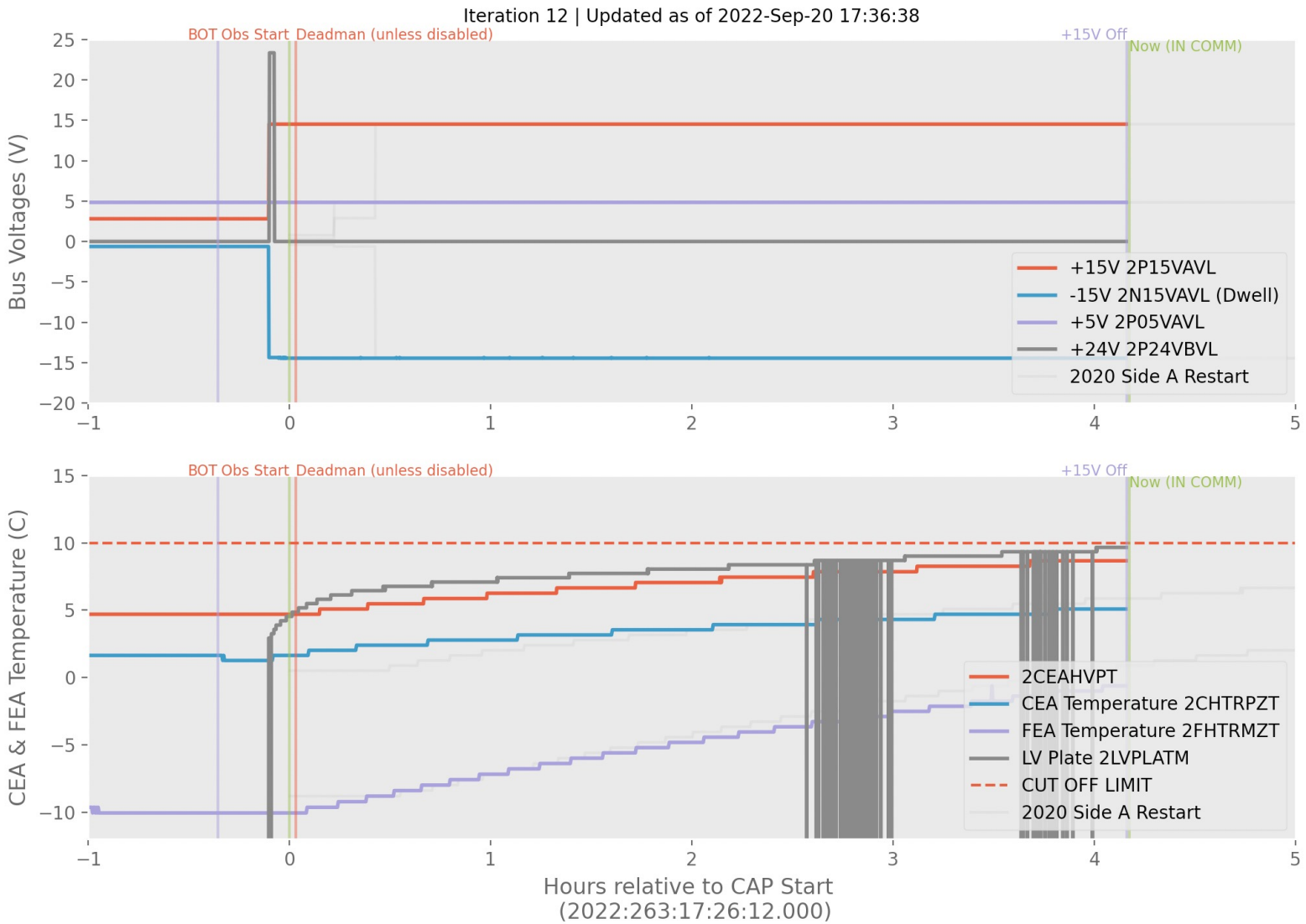
HRC thermal model – historical performance



HRC thermal model – solar heating versus pitch angle



2CEAHVPT as a proxy for 2LVPLATM



- 2LVPLATM is located on HRC LV board – only available when ±15V is powered and nominal
  - 2LVPLATM is susceptible to secondary science corruption
- 2CEAHVPT is located on the HVPS bracket and close to LVPS board
- Heating rate of HVPS bracket is functionally similar to heating of LVPS board (lower panel, red curve vs. gray curve)
- Data are from fourth checkout observation

Products Requiring Revision (and current status)

- SOT: check_hrc.pl
  - Requires reverting code to pre-August 2020 version
  - Updates to error reporting of antico shield activation (no longer needed)
  - Status: under testing
- SOT: hrcmon.pl
  - Updates to constants to convert digital values based on fit parameters in P016 TDB
  - Status: under testing
- FOT: SCS 104
  - Add commands to power down 15V LVPS
  - Status: complete
- FOT: SCS 87/88
  - Update to set HVPS to 0 steps when activated
  - Status: complete
- FOT/SOT: P016 TDB changes
  - Status: Changes being identified
- FOT: SOH SOP
  - Add instructions to power down LVPS under certain conditions
  - Status: SOT has provided text and procedure
- FOT: HRC ATSs
  - Modify and develop new ATSs for HRC planning
  - Status: SOT/FOT are testing new ATSs
- FOT: Safing response/return to science SOPs
  - Modify SOPs to set HRC HVPS steps to 0 steps for **both** detectors
  - Status: to be redlined
- FOT: Incorporate HRC thermal model into FOT tools
  - Status: testing
- SOT: Incorporate cea_checker.py into load review tools
  - Status: testing
- HRC disabling procedure
  - Status: CAP and/or SOP under consideration